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EXAMINER	
NGUYEN, C.	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 1

Application Number: 09/161,196
Filing Date: September 25, 1998
Appellant(s): Frank Hintermaier

Markus Nolff
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 06-08-01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Claim 1 is independent. Claims 3, 5 and 7-12 depend on claim 1 and they stand or fall with claim 1.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,566,045	Summerfelt	Oct. 15, 1996

5,691,219	Kawakubo et al.	Nov. 25, 1997
6,015,997	Hu et al.	Jan. 18, 2000
5, 705,685	Lyons et al.	Jan. 6, 1998
5,990,348	Lyons et al.	Nov. 23, 1999
6,043,184	Karmakar	Mar. 28, 2000
6,060,419	Wijesekera et al.	May. 9, 2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Summerfelt et al. (US 5,566,045).

Regarding claims 1, 7, 8, 9, Summerfelt et al. discloses a capacitor structure in an integrated semiconductor device comprising: a semiconductor substrate (30); a first electrode (34, a platinum group materials. See Summerfelt et al.'s col.10) connected to

a doped region (44), capacitor dielectric layer (38, a BST layer with a dielectric constant greater that 100. See Summerfelt et al.'s col.11) formed on the first electrode; a barrier layer (52, a GaAs layer. See Summerfelt et al.'s col.13) which is a compound of a transition element (Ga) and As formed below the capacitor dielectric layer; a second electrode formed on the capacitor dielectric layer. See Summerfelt et al.'s Fig.12.

Claims 1, 3-5, and 7-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Kawakubo et al. (US 5,691,219).

Regarding claims 1, 3, 7, 8, 9, 10, 11, Kawakubo et al. discloses a capacitor structure in an integrated semiconductor device comprising: a semiconductor substrate (1) having a doped region (6b) therein; a first electrode (13, a platinum alloy) connected to the doped region through a connection structure (11, a phosphorus-doped polysilicon layer. See Kawakubo et al.'s col.7 lines 39-43); a capacitor dielectric layer (14, a BST layer with a dielectric constant greater than 100. See Kawakubo et al.'s col.8 lines 5-8) formed on the first electrode; a barrier layer (12, a layer of transition metal such as Ti or Ta. See Kawakubo et al.'s col.7 lines 55-60) formed below the capacitor dielectric layer; a second electrode (14) formed on the capacitor dielectric layer. See Kawakubo et al.'s Fig.4E.

Kawakubo et al. does not explicitly teach that the barrier is a compound of a transition element and phosphorus as the barrier; however, this barrier layer is taken to